Timing Hazards

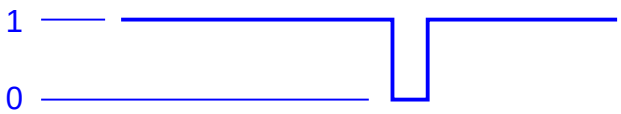
Do to timing delays, the *transient behavior* of a logic circuit may differ from what is predicted by a *steady-state* analysis. A circuit's output may produce a glitch at a time when steady-state analysis predicted that the output should not change. A hazard exist when a circuit has the possibility of producing a glitch.

Types of Hazards…

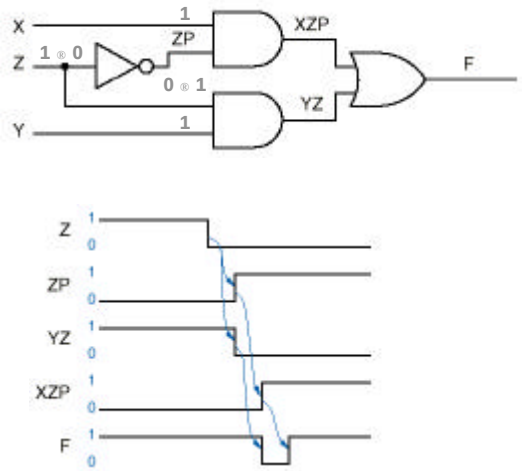
- Static – 1 Hazard
- Static – 0 Hazard
- Dynamic Hazard

Static – One Hazard

A static-1 hazard is a pair of input combinations that : (a) differ in only one input variable and (b) both give a give a 1 output; such that it is possible for a momentary 0 output to occur during a transition in the differing input variable.

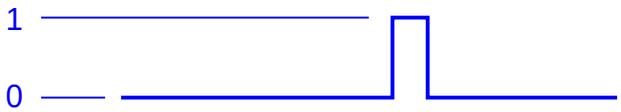


Static – 1 Hazard Example

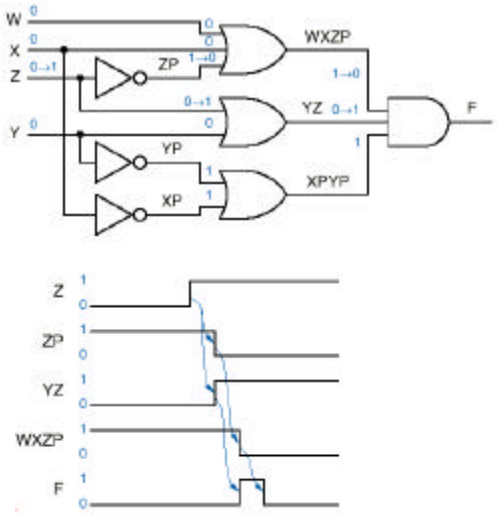


Static – Zero Hazard

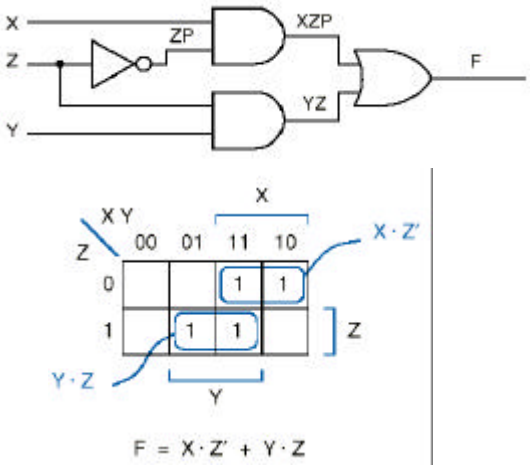
A static-0 hazard is a pair of input combinations that : (a) differ in only one input variable and (b) both give a give a 0 output; such that it is possible for a momentary 1 output to occur during a transition in the differing input variable.



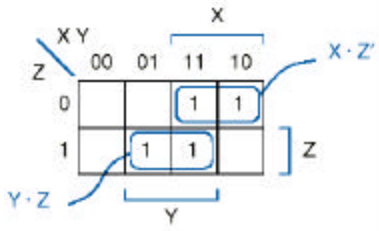
Static – 0 Hazard Example



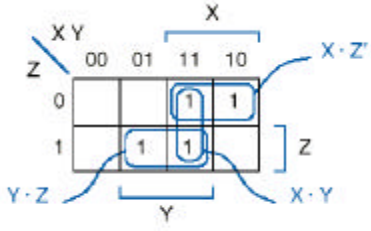
Finding Static Hazards w/ K-Maps



"Covering" A Hazard

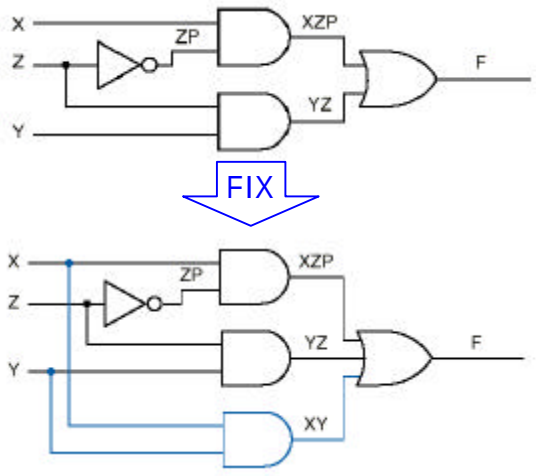


$F = X \cdot Z' + Y \cdot Z$



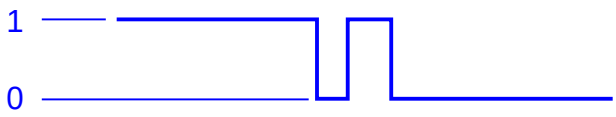
$F = X \cdot Z' + Y \cdot Z + X \cdot Y$

Hazard Free Circuit



Dynamic Hazard

A dynamic hazard is the possibility of an output changing more than once as the result of a single input transition. A dynamic hazard can occur if there are multiple paths with different delays from the changing input to the changing output



Dynamic Hazard Example