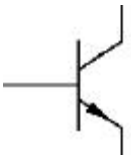
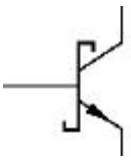
Bipolar Junction Transistors

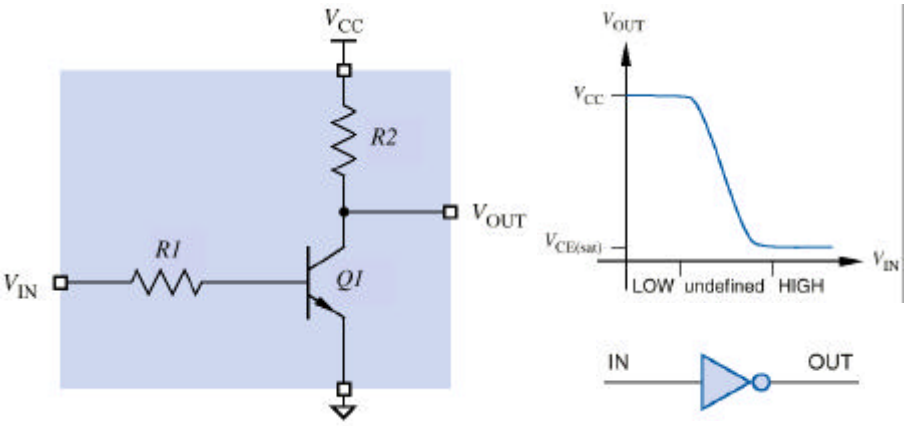
NPN Transistor



Schottky Transistor

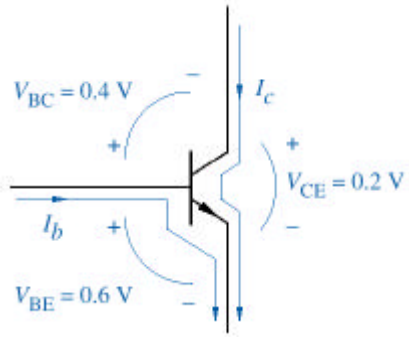


Standard TTL Logic Inverter (model)

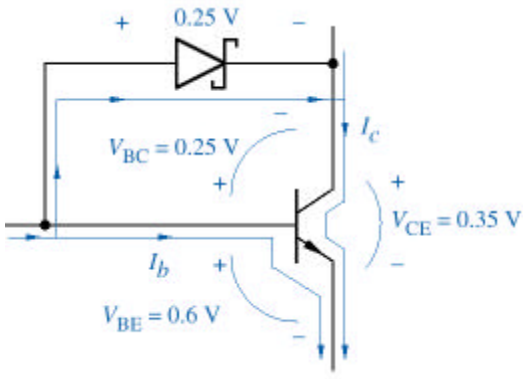


Problem With Standard TTL

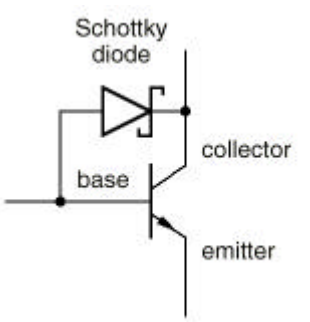
- Transistor Storage Time
- Significant Propagation Delay



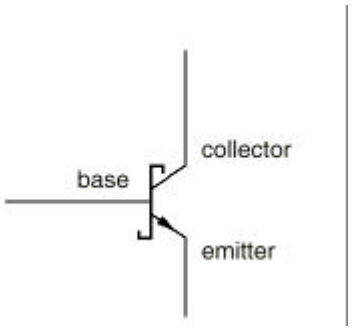
Schottky-Clamped Transistor



Schottky Transistor

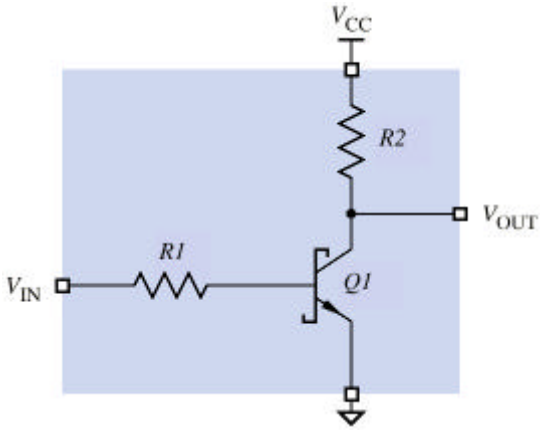


Schottky-Clamped Transistor

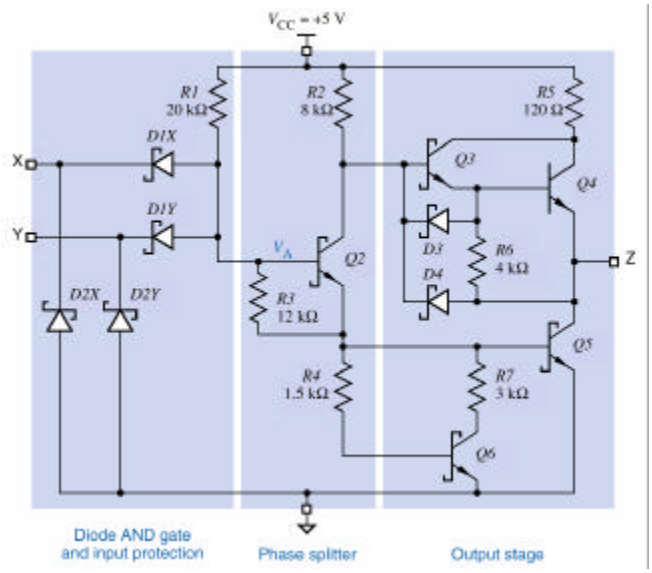


Schottky Transistor Symbol

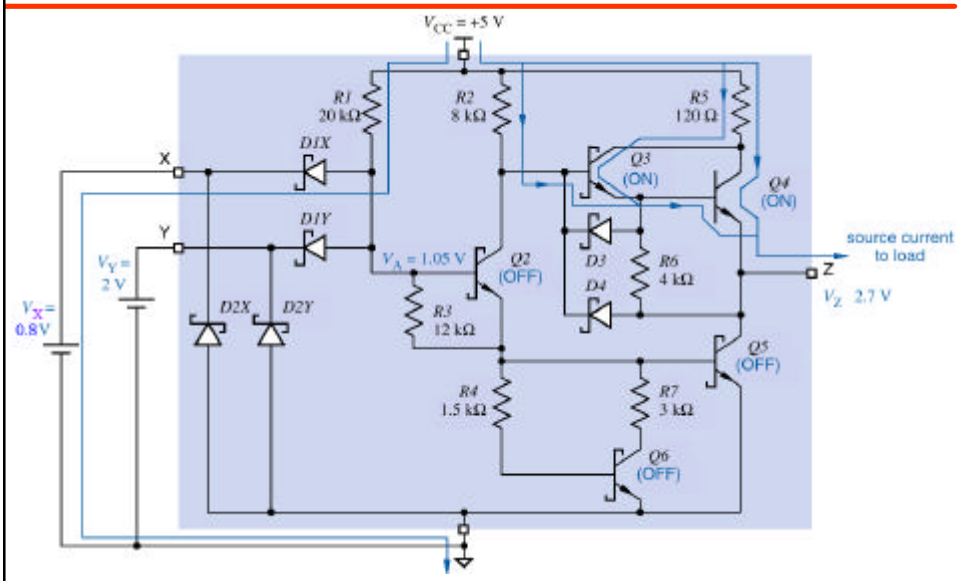
Schottky TTL Logic Inverter (model)



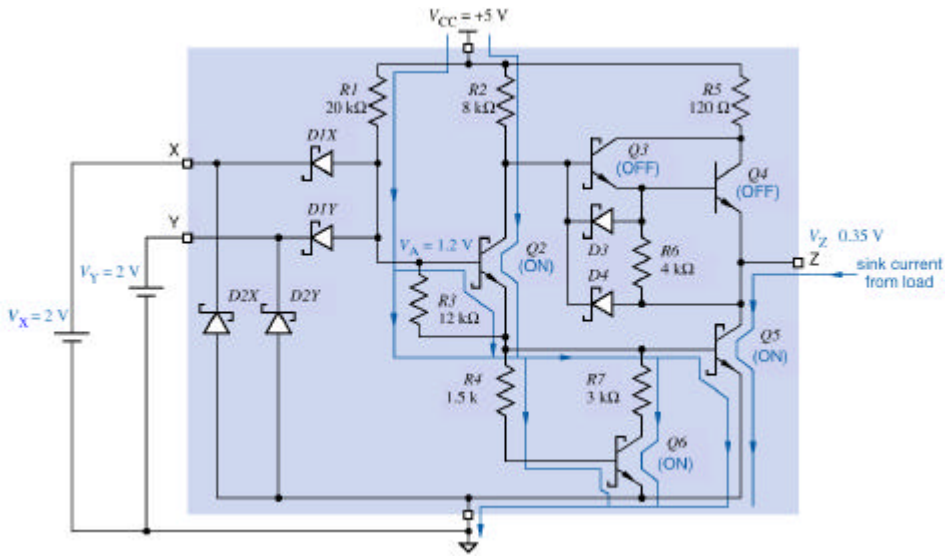
TTL NAND Gate (74LS00)



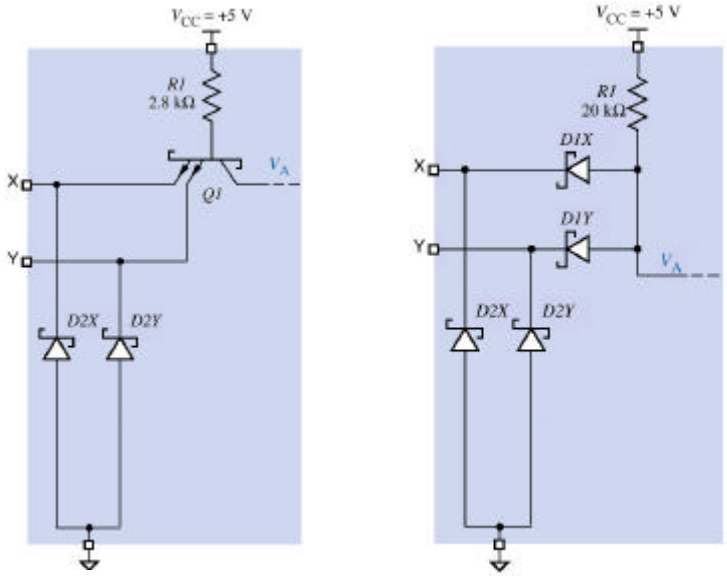
NAND Gate (74LS00) : Output High



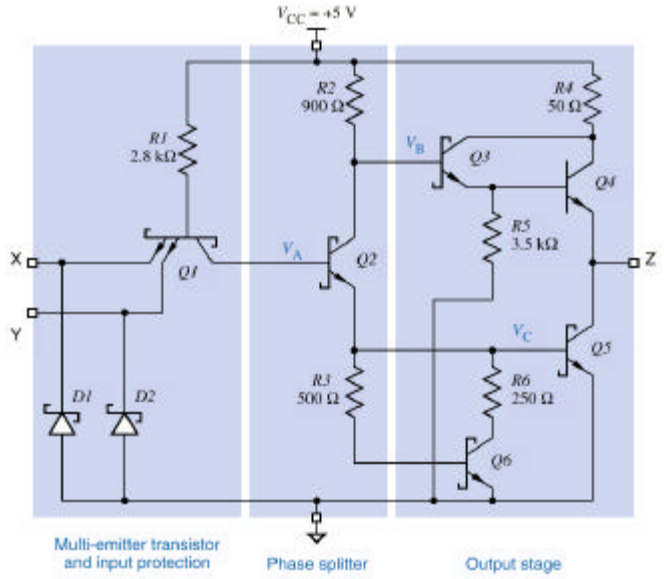
NAND Gate (74LS00) : Output Low



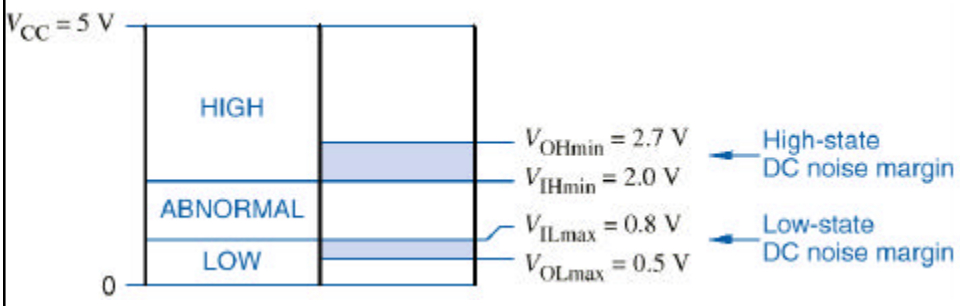
Multi-Emitter Transistor



74LS00 With Multi-Emitter Input Transistor

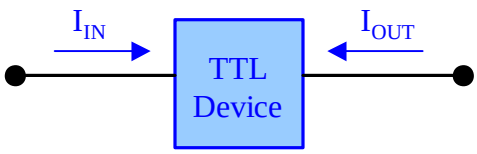


Logic Levels and Noise Margins



Fanout

- The *fanout* of a logic gate is the number of inputs that the gate can drive without exceeding its worst-case loading specifications.
- *Fanout* must be examined for both possible output states.
- TTL input or output lead is defined to be positive if the current actually flows into the lead, and negative if the current flows out of the leads.

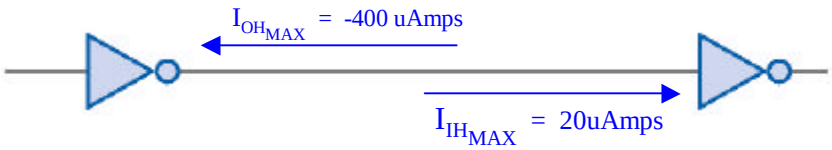


Current Drive Capability

- $I_{IL_{MAX}}$: The maximum current that an input requires to pull it LOW. Since current flows out of a TTL input in the LOW state, $I_{IL_{MAX}}$ has a negative value. Approximately –0.4 mAmps for most TTL inputs.
- $I_{IH_{MAX}}$: The maximum current that an input requires to pull it HIGH. Since current flows into a TTL input in the HIGH state, $I_{IH_{MAX}}$ has a positive value. Approximately 20uAmps for most TT inputs.
- $I_{OL_{MAX}}$: The maximum current that the output can sink in the LOW state while still maintaining an output voltage no greater then $V_{OL_{MAX.}}$ Since current flows into the output, $I_{OL_{MAX}}$ has a position value. Approximately 8 mAmps for most TTL outputs.
- $I_{OH_{MAX}}$: The maximum current that the output can source in the HIGH state while still maintaining an output voltage no less then $V_{OH_{MIN.}}$ Since current flows out of the output, $I_{OH_{MAX}}$ has a negative value. Approximately –400 uAmps for most TTL inputs.

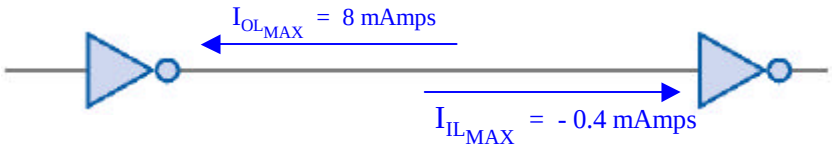
Asymmetrical TTL Outputs

High Output



$Fanout_{HIGH}$ = 400uAmp / 20 uAmp = 20

Low Output

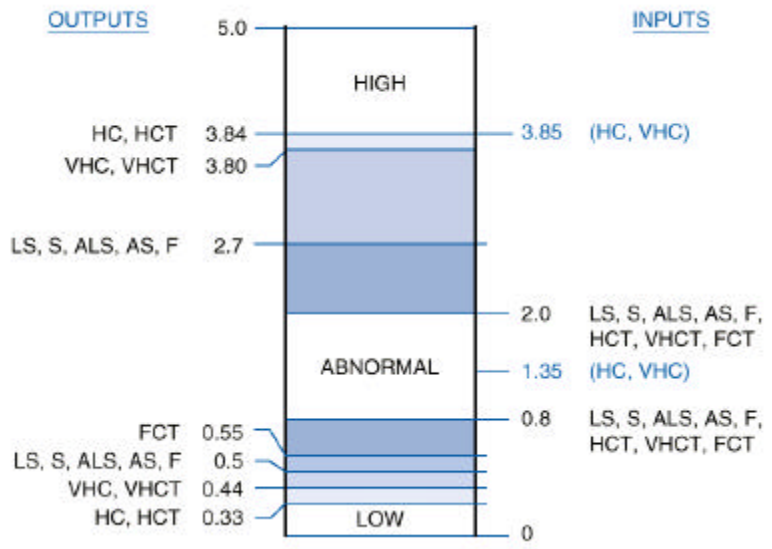


$Fanout_{LOW}$ = 8 mAmp / 0.4 mAmp = 20

TTL Families

- 74xx : Introduced by Sylvania in 1963, Popularized by TI
- 74Hxx : High Speed TTL, Reduce propagation delay achieved by lowing resistor values at the expense of increased power consumption.
- 74Lxx : Low Power TTL, Reduce power consumption achieved by raising resistor values to at the expense of increased propagation delay.
- 74Sxx : Schottky TTL, Reduced propagation delay achieved by using Schottky transistors.
- 74LSxx : Lower Power Schottky TTL, Reduced propagation delay and reduced power consumption achieved by using Schottky transistors with higher resistor values
- 74ASxx : Advanced Schottky and 74ALSxx : Advanced Lower Power Schottky.

Logic Levels – CMOS & TTL (specific)



Characteristics Of TTL Families

Table 3-11, page 167

TTL NOR Gate (74LS02)